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| 10/608,015 | 06/30/2003 | Masayuki Kabasawa | HITA.0406 | 1937 |

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| EXAMINER | |
|---|---|
| ALROBAYE, IDRISS N | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2183 | |

DATE MAILED: 10/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/608,015 | KABASAWA ET AL. | |
| | Examiner | Art Unit | |
| | Idriss N. Alrobaye | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *6-30-2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06-30-2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. This action is responsive to communications through the applicant's application filed on 06/30/2003.

Claims 1-15 are presented for examination

### *Specification*

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

3. The disclosure is objected to because of the following informalities:

Fig. 10 is not described in the "Brief Description of the Drawing" section.

The "Detailed Description of the Preferred Embodiments" contains typos. As for example in page 10, line 3, "...when the CPU 2" should be corrected to "...when the CPU 4". In page 23, line 20-21, "CPU 1" should be "CPU 4" and "accelerator 10" should be "accelerator 2". The specification has not been checked to the extent necessary to determine the present of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### *Claim Objections*

4. The use of "instruction translator" is vague and unclear. The examiner suggests modifying the claims to differentiate between hardware and software translators.

Perhaps to change it to "hardware instruction translator" and "software instruction translator."

Claim 1, line beginning with "instruction translator", it is unclear to whether it is referring to the software or hardware translator. The examiner assumes that it's referring to the hardware instruction translator. In line beginning with "wherein said information processing device", the examiner suggests to change it to "wherein said software instruction translator". Also, in claim 1, the term "redefine" is vague, thus the examiner assumes the term refers to reconfiguration. Appropriate correction and clarification is required.

Claim 5, "...wherein said software is described with said first instruction set" it is vague, the examiner assumes the claim means that using the software to translate the second instruction group to be equivalent to the first instruction set. Appropriate clarification is required.

Claim 8, the examiner assumes the "first area" as the base address, the "second area" as the length of the array and the "third area" as the index. Appropriate clarification is required.

### *Claim Rejections - 35 USC § 102*

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Seal et al. US PG-Pub 2002/0188825 (hereinafter Seal).

As per claim 1, Seal teaches an information processing device, comprising:

an instruction execution block for executing a first instruction set as a specific instruction (see e.g. paragraph [0013], wherein the second instruction set (e.g. Java bytecode) is equivalent to "a first instruction set as a specific instruction". Also, see paragraph [0062]); and

an instruction translator (Fig. 1, element 6) for translating an instruction included in a first instruction group of a second instruction set to said first instruction set to be supplied to said instruction execution block (see e.g. paragraph [0062], bytecode translation hardware. See also Fig. 18, element 322, Jazelle bytecode accelerator. Note that the examiner assumes the "instruction translator" is a hardware component as it is defined in the specification),

wherein said information processing device, when receiving an instruction included in a second instruction group of the second instruction set, which is not translated by said instruction translator, translates the instruction included in the second instruction group to the first instruction set with use of software so as to be executed by said instruction execution block (see e.g. paragraph [0064] and [0065]), and

wherein said instruction translator has a first storage area for storing an information to be able to redefine whether each of the instruction of the second instruction set is included in the first instruction group or the second instruction group (see e.g. paragraph [0143] and Fig. 18, elements 326, 328 and 330. The translation table 326 requires programming for each Java Virtual Machine for which it is desired to execute Java bytecode. Thus, through programming the translation table would redefine the bytecode with the help of the configuration data register 328 and the operating system control register 330. Also, see paragraph [0142] on reconfiguration).

As per claim 2, Seal teaches the invention as claimed above. Seal further teaches the information processing device according to claim 1, wherein the instructions of the second instruction set is classified into a plurality of instruction categories, and wherein the first storage area stores the information according to each of the plurality of the instruction categories (see e.g. paragraph [0087] and Fig. 7, wherein the shown bytecode bindings is equivalent to categories).

As per claim 3, Seal teaches the invention as claimed above. Seal further teaches the information processing device according to claim 2, wherein each of said plurality of instruction categories includes any one of a local variable access instruction group, an array access instruction group, a 32-bit operation instruction group, a 64-bit operation instruction group, a floating decimal point instruction group, a stack handling

instruction group, a subroutine jump/return instruction group, and a flow control instruction group (see e.g. paragraph [0151] for floating point operation).

As per claim 4, Seal teaches the invention as claimed above. Seal further teaches the information processing device according to claim 1, wherein said instruction translator, when receiving the instruction of the second instruction set, refers to the information stored in the first storage area to change the inputted instruction to a first instruction format one if it is included in the first instruction group or to let the software to execute the inputted instruction if it is included in the second instruction group (see e.g. paragraph [0064], [0065]. Also, see paragraph [0089-0091], in which the translation is explained in details).

As per claim 5, Seal teaches the invention as claimed above. Seal further teaches the information processing device according to claim 1, wherein said software is described with said first instruction set (the examiner assumes the claim means that using the software to translate the second instruction group to be equivalent to the first instruction set, see e.g. paragraph [0065])

As per claim 6, Seal teaches the invention as claimed above. Seal further teaches the information processing device according to claim 1, wherein said instruction translator includes:

a controller for storing an operation code defined in a first version of the software and controlling its processing and a second storage area for changing a relationship between the operation code stored in said controller and its processing when the software version is upgraded (see e.g. paragraph [0143] and Fig. 18, elements 326,328, and 330, wherein translation table is equivalent to a controller and as is described, it requires programming for each Java Virtual Machine for which it is desired to execute Java bytecode).

As per claim 7, Seal teaches the invention as claimed above. Seal further teaches the information processing device according to claim 6, wherein said instruction translator includes a third storage area for storing information used to dispose an array or field defined in the second instruction set in a memory so as to be redefined (see e.g. paragraph [0095] and [0019]).

As per claim 8, Seal teaches the invention as claimed above. Seal further teaches the information processing device according to claim 7,

wherein the third storage area includes:

a first area for storing an offset value for between the start address of said memory and the start entry of an array when said array is defined in the second instruction set and disposed in said memory (the examiner assumes this feature means the base address, see e.g. paragraph [0019] and [0067]);

a second area for storing an offset value for between the start address of said memory and a field for storing a length of said array when said array is to be disposed in said memory (see e.g. paragraph [0093] and [0095]); and

a third area for storing an offset value for between the start address of said memory and the start entry of said field when a field defined in said second instruction set is disposed in said memory (the examiner assumes this feature means the index, see e.g. paragraph [0019] and [0067]).

As per claim 9, Seal teaches the invention as claimed in claim 1 above. Seal further teaches the instruction translator to include:

a controller for storing an operation code defined by the first version of said software and its processing; and a second storage area for changing a relationship between said operation code stored in said controller and its processing when the version of the software is upgraded (see e.g. paragraph [0143], wherein the translation table is equivalent to a controller. See also Fig. 18, the elements inside the bytecode accelerator 322).

As per claim 10, Seal teaches the invention as claimed above. Seal further teaches the information processing device according to claim 9, wherein said controller also stores an operation code defined in the second version of the software and its processing in addition to the relationship between the operation code defined by the first version of the software program and its processing, and wherein said second storage

area includes an area for specifying a relationship between said controller and the first or second version so as to be redefined (see e.g. paragraph [0006], it talks about the prior art of updating a new version of java byte code. Paragraph [0142-0143] explains reconfiguration of Java acceleration hardware. Also, see paragraph [0097], where it talks about different programmable mapping hardware interpreters support different sets of operation values).

As per claim 11, Seal teaches the invention as claimed above. Seal further teaches the information processing device according to claim 9, wherein said controller stores a relationship between an operation code defined in the first version of the software and its processing (see e.g. paragraph [0142-0143]),

wherein said second storage area includes:

a first area for specifying that part of the relationship between an operation code stored in said controller and its processing is invalidated so as to be redefined (see e.g. paragraph [0142-0143], wherein a configuration invalid indicator associated with the Java acceleration hardware to an invalid state is equivalent to invalidate processing to be redefined); and

a second area for storing a new operation code for the processing invalidated by said first area so as to be redefined (see e.g. paragraph [0142-143], the translation table requires programming for each Java Virtual Machine for which it is desired to execute Java bytecode is equivalent to storing a new operation code for processing).

As per claim 12, Seal teaches the invention as claimed above. Seal further teaches the information processing device according to claim 9,

wherein said second instruction set is the Java bytecode (see e.g. paragraph [0013]),

wherein said software is a software virtual machine that executes said Java bytecode in said information processing device (see e.g. paragraph [0141]), and

wherein said second storage area can reset a relationship between an operation code of an extended bytecode of said Java bytecode and its processing content (see e.g. paragraph 143, wherein the translation table requires programming for each Java Virtual Machine for which it is desired to execute Java bytecode. Thus, this can be updated for each Virtual Machine for which it is desired to execute Java bytecode, it can reset a relationship between an operation code of an extended bytecode and its processing content).

As per claim 13, Seal teaches an information processing device, comprising:

an instruction execution block for executing a specific instruction (see e.g. paragraph [0062]); and

an instruction translator (Fig. 1, element 6) for translating an instruction included in a first instruction group of the Java bytecode to said specific instruction to be supplied to said instruction execution block (see e.g. paragraph [0062]),

wherein said information processing device, when receiving an instruction included in a second instruction group of said Java bytecode, which is not translated by

said instruction translator, translates said received instruction to the specific instruction with use of a software virtual machine so as to be executed by said instruction execution block (see e.g. paragraph [0064-0065]), and

wherein said instruction translator includes:

a first storage area for redefining classification of said Java bytecode into said first instruction group and said second instruction group (see e.g. paragraph [0089] and [0090]);

a second storage area for redefining a relationship between an operation code of said Java bytecode and its processing content (see e.g. paragraph [00142] and [00143]); and

a third storage area for redefining information used to dispose an array or field defined in said Java bytecode in a memory (see e.g. paragraph [0095] and [0143]).

As per claim 14, Seal teaches the invention as claimed above. Seal further teaches the information processing device according to claim 13, wherein said information processing device writes a predetermined value in said first to third storage areas respectively, thereby coping with to the version upgrading of said software virtual machine (see e.g. paragraph [0006], it talks about the prior art of updating a new version of java byte code. Paragraph [0142-0143] explains reconfiguration of Java acceleration hardware. Also, see paragraph [0097], where it talks about different programmable mapping hardware interpreters support different sets of operation values).

As per claim 15, Seal teaches the invention as claimed above. Seal further teaches the information processing device according to claim 14, wherein said Java bytecode is classified into a plurality of instruction categories, and wherein the first storage area stores the information according to each of the plurality of the instruction categories (see e.g. paragraph [0087] and Fig. 7, wherein the shown bytecode bindings is equivalent to categories).

***Conclusion***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Nevill et al. shows system having mixed hardware and software based instruction execution, US Patent 2002/0069402.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Idriss N. Alrobaye whose telephone number is 571-270-1023. The examiner can normally be reached on Mon-Fri from 8:00 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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